Form PTO-1449 (modified)	Atty. Docket No. 10830.0110.NPUS00	Serial No.
List of Patents and Publications for Applicant's INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	**Applicant** Jean-Pierre Bono	
	Filing Date:	**Group:**

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1	2003/ 0018691 A1	01/23/2003	Bono	709	106	06/29/2001
	A2	6,604,182	08/05/2003	Sexton et al.	711	170	02/25/2000
	A3	6,594,735	07/15/2003	Baker et al.	711	147	12/28/1998
	A4	6,430,667	8/6/2002	Loen	711	202	04/13/2000
	A5	6,381,682	4/30/2002	Noel et al.	711	153	06/10/1998
	A6	6,324,581	11/27/2001	Xu et al.	709	229	03/03/1999
	A7	6,314,501	11/06/2001	Gulick et al.	711	153	12/18/1998
	A8	6,240,501	05/29/2001	Hagersten	711	202	09/04/1998
	A9	6,182,089	01/30/2001	Ganapathy et al.	707	206	09/23/1997
	A10	6,112,286	08/29/2000	Schimmel et al.	711	208	09/19/1997
	A11	6,003,123	12/14/1999	Carter et al.	711	207	02/10/1998
	A12	5,893,140	04/06/1999	Vahalia et al.	711	118	11/13/1996
	A13	5,737,605	04/7/1998	Cunningham et al.	395	670	10/08/1996
	A14	4,691,280	09/01/1987	Bennett	364	200	02/18/1986
	A15	4,445,174	04/24/1984	Fletcher	364	200	03/31/1981

Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	EMC Celerra SE5 File Server, EMC Corporation, Hopkinton, MA, 2002, 2 pages.

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EXAMINER: INITIAL IF REFERENCE CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

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Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C2	"Celerra File Server in the E-Infostructure," EMC Corporation, Hopkinton, MA, 2000, 9 pages.
	C3	"Celerra File Server Architecture for High Availability," EMC Corporation, Hopkinton, MA, 1999, pp. 1-7.
	C4	"*MultiProcessor Specification Version 1.4*," May 1997, Intel Corporation, Mt. Prospect, IL, 1993-1997, 1-1 to 5-8, A-1 to E-6.
	C5	Helen S. Raizen and Stephen C. Schwarm, "*Building a Semi-Loosely Coupled Multiprocessor System Based on Network Process Extension*," Prime Computer, Inc., Framingham, MA, Pre-Publication Copy, January 29, 1991, pp. 1-17.
	C6	Morioka et al., "Design and Evaluation of the High Performance Multi-Processor Server," IEEE International Conference on Computer Design: VLSI in Computers and Processors, IEEE Computer Society Press, Los Alamitos, CA 1994, pp. 66-69.
	C7	"Intel Xeon Processor: Unparalleled Value and Flexibility for Small and Medium Business Server Applications," Intel Corporation, Santa Clara, CA, 2002, 4 pages.
	C8	"Intel Server Board SE7500WV2;" Intel Corporation, Santa Clara, CA, 2002, 6 pages.
	C9	"Building Cutting-Edge Server Applications: Intel Xeon Processor Family Features the Intel NetBurst Microarchitecture with Hyper-Threading Technology;" White Paper, Intel Corporation, Santa Clara, CA, 2002, 10 pages.
	C10	Levy & Eckhouse, Jr., Computer Programming and Architecture – The VAX-11, Digital Equipment Corporation, Bedford, Mass., 1980, pp. 247-253, 356-360.
	C11	Intel 80386 Reference Programmer's Manual, Table of contents (4 pages),Chapter 2.1 Memory Organization and Segmentation (2 pages), Chapter 5 Memory Management (2 pages), Chapter 5.1 Segment Translation (6 pages), Chapter 5.2 Page Translation (4 pages), Chapter 5.3 Combining Segment and Page Translation (3 pages), , http://www7.informatik.uni-erlangen.de, Friederich-Alexander-Universitat, Erlangen-Nurnberg, Germany.
	C12	Addendum – Intel Architecture Software Developer's Manual, Vol. 3: System Programming Guide, Intel Corp., Santa Clara, CA 1997, pp. 3-1 to 304 and 9-1 to
	C13	The IA-32 Intel® Architecuter Software Developer's Manual, Vol. 3, System Programming Guide, Intel Corp., Santa Clara, CA, 2004, Table of Contents and pp. 3-1 to 3-38.

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Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

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	C14	"PAE36 and Linux Virtual Memory System – The Need for PAE32," www.prism.gatech.edu, Georgia Institute of Technology, Atlanta, Georgia, printed 12/5/2003, 4 pages.
	C15	" Windows – Operating System and PAE Support," www.microsoft.com, Microsoft Corp., Bellevue, WA, printed 12/5/2003, 6 pages.
	C16	"Physical Address Extension X86 Overview," www.microsoft.com, Microsoft Corp., Bellevue, WA, printed 12/5/2003, 1 page.
	C17	"Intel Physical Address Extensions (PAE) in Windows 2000," http://support.microsoft.com, Microsoft Corp., Bellevue, WA, printed 12/5/2003, 1 page.
	C18	"PAE Design," www.microsoft.com, Microsoft Corp., Bellevue, WA, printed 12/5/2003, 3 pages.
	C19	"PAE Memory and Windows," www.microsoft.com, Microsoft Corp., Bellevue, WA, printed 12/5/2003, 10 pages.
	C20	"How to Configure the Paged Address Pool and System Page Table Entry Memory Areas," http://support.microsoft.com, Microsoft Corp., Bellevue, WA, printed 12/5/2003, 4 pages.
	C21	"Scaling Out Verses Scaling Up with Intel Physical Addressing Extensions (PAE)," http://support.microsoft.com, Microsoft Corp., Bellevue, WA, printed 12/5/2003, 1 page.
	C22	"Physical Address Extension (PAE) - PAE Memory Support," www.osr.com, OSR Open Systems Resources, Inc., Amherst, NH, printed 12/05/2003, 6 pages.

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